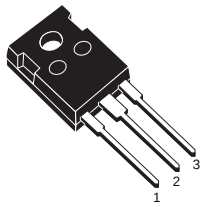
STW18NK80Z

N-CHANNEL 800V - 0.34Ω - 19A TO-247

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STW18NK80Z	800 V	< 0.38 Ω	19 A	350 W

- TYPICAL $R_{DS}(on)$ = 0.34 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

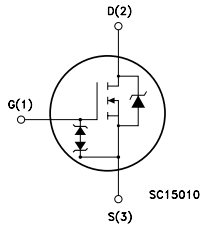


TO-247

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW18NK80Z	W18NK80Z	TO-247	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	800	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	19	A
I_D	Drain Current (continuous) at T_C = 100°C	12	A
I_{DM} (•)	Drain Current (pulsed)	76	A
P_{TOT}	Total Dissipation at T_C = 25°C	350	W
	Derating Factor	2.4	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(•) Pulse width limited by safe operating area
(1) I_{SD} ≤19A, di/dt ≤300A/µs, V_{DD} ≤ 800V , T_j ≤ $T_{JMAX.}$
(*) Limited only by maximum temperature allowed

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.36	°C/W
Rthj-amb T_l	Thermal Resistance Junction-ambient Max Maximum Lead Temperature For Soldering Purpose	50 300	°C/W °C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	19	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	700	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 150 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 10 A		0.34	0.38	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 10 A		19		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		6100 500 100		pF pF pF
$C_{oss\ eq.}$ (3)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 640V		240		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 400 V, I_D = 9 A R_G = 4.7Ω V_{GS} = 10 V (Resistive Load see, Figure 3)		46 32 140 32		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 640V, I_D = 18 A, V_{GS} = 10V		192 34 102	250	nC nC nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				19 76	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 19 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 18 A, di/dt = 100A/µs V_{DD} = 40 V, T_j = 25°C (see test circuit, Figure 5)		920 11 24		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 18 A, di/dt = 100A/µs V_{DD} = 40 V, T_j = 150°C (see test circuit, Figure 5)		1160 15 25.8		ns µC A

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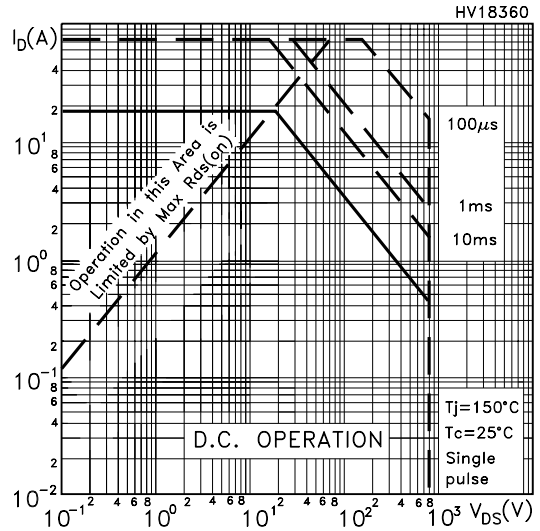
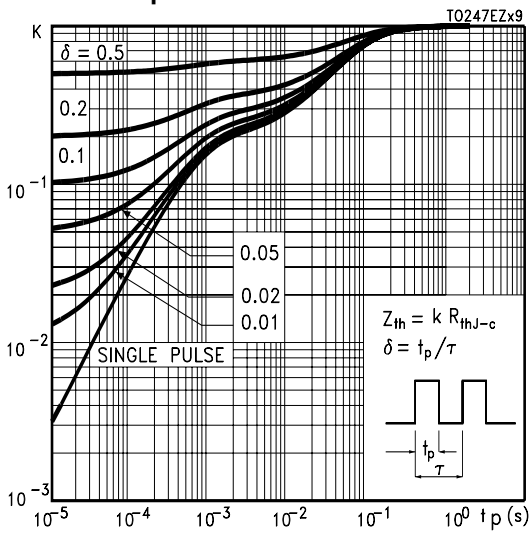
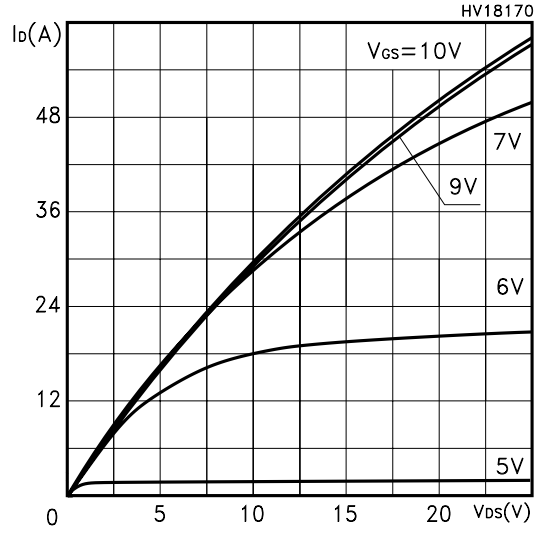
Safe Operating Area



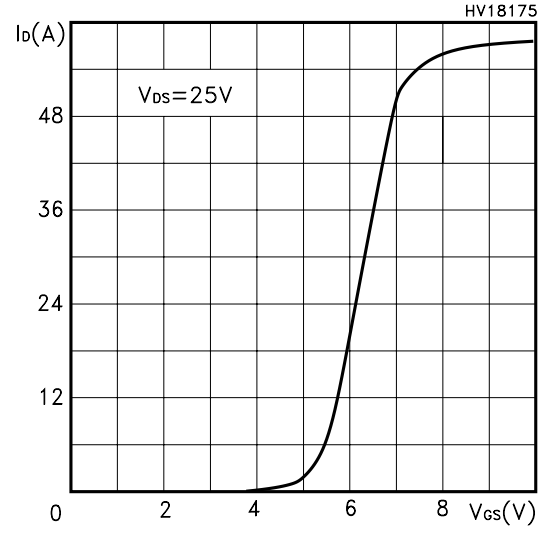
Thermal Impedance



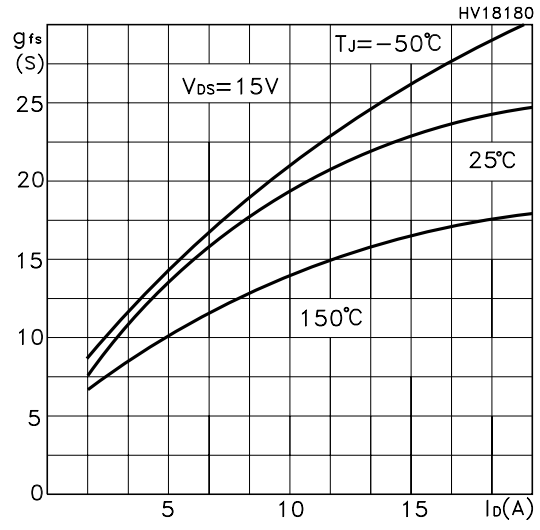
Output Characteristics



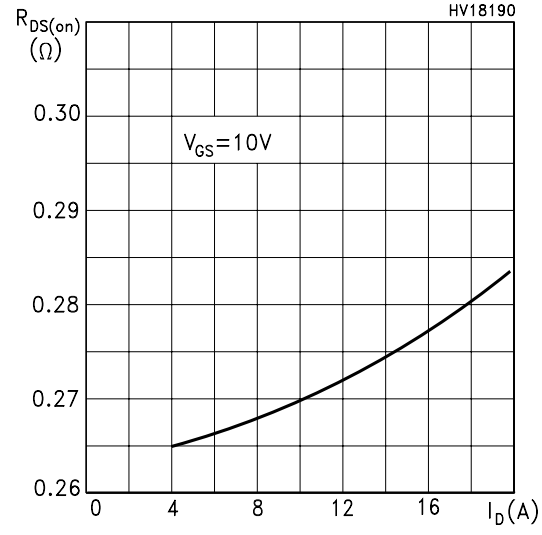
Transfer Characteristics



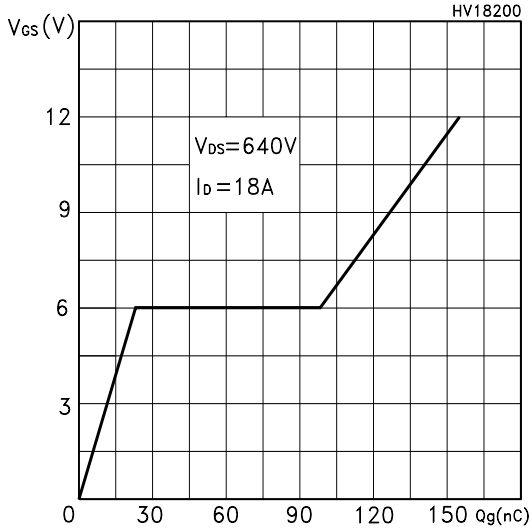
Transconductance



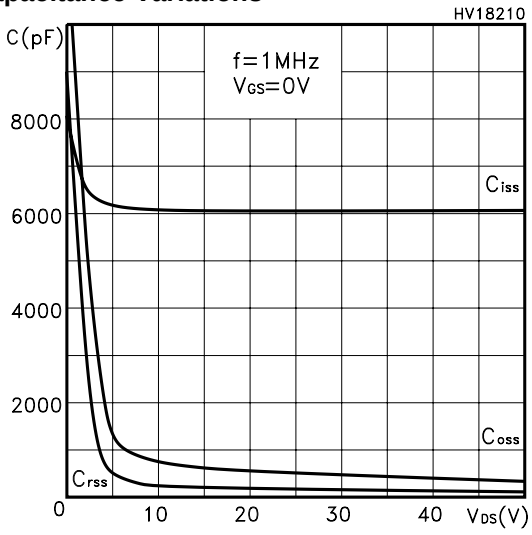
Static Drain-source On Resistance



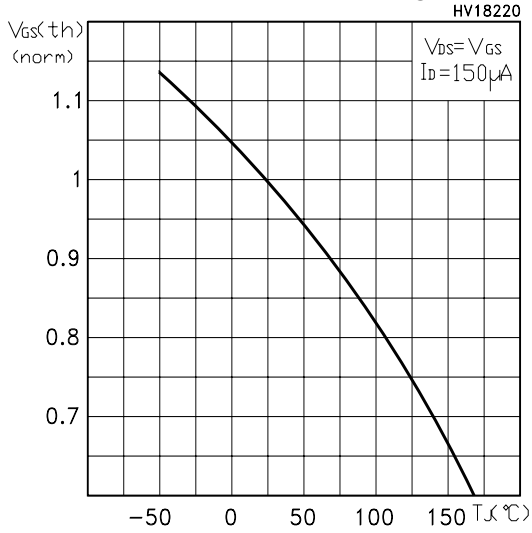
Gate Charge vs Gate-source Voltage



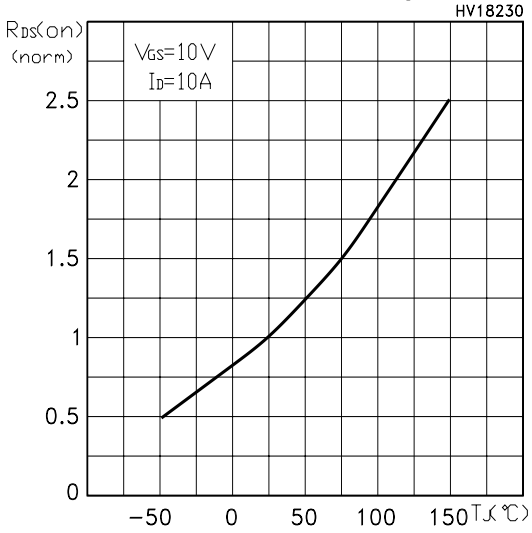
Capacitance Variations



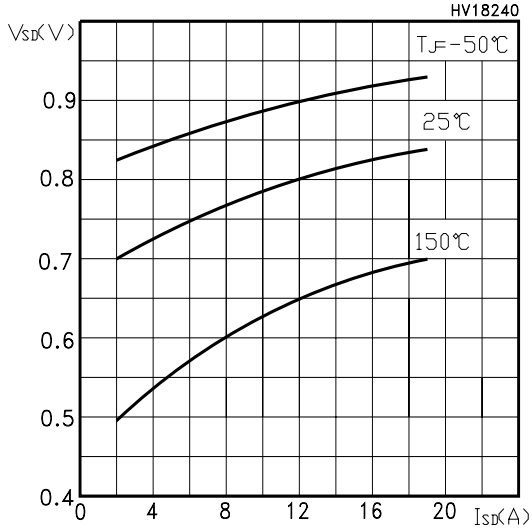
Normalized Gate Thereshold Voltage vs Temp.



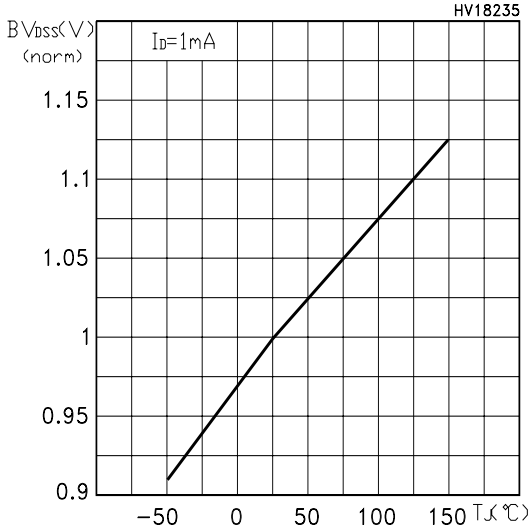
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature

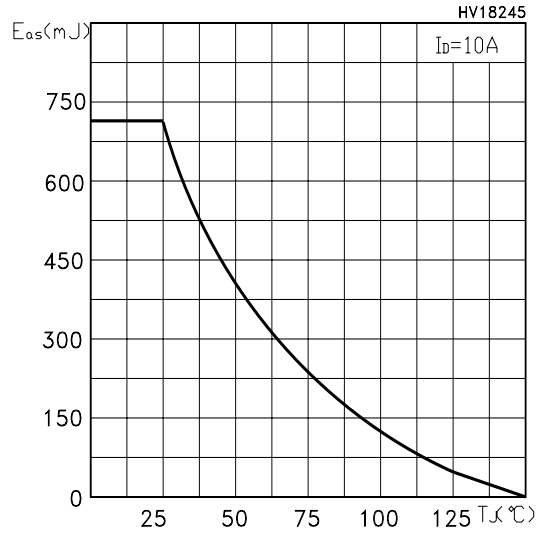


Fig. 1: Unclamped Inductive Load Test Circuit

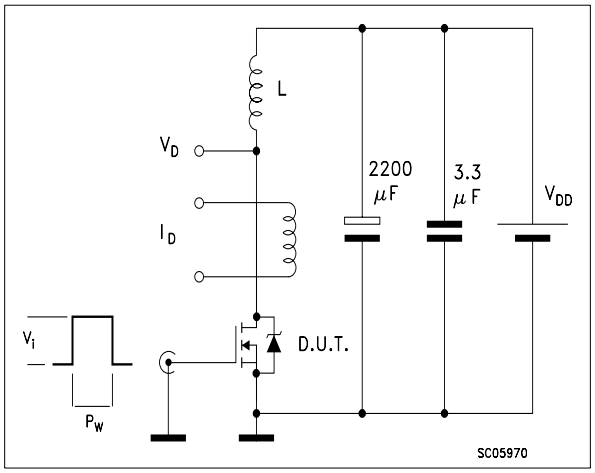


Fig. 2: Unclamped Inductive Waveform

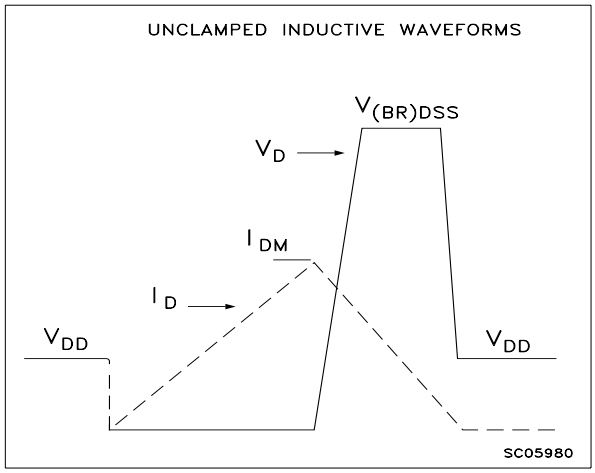


Fig. 3: Switching Times Test Circuit For Resistive Load

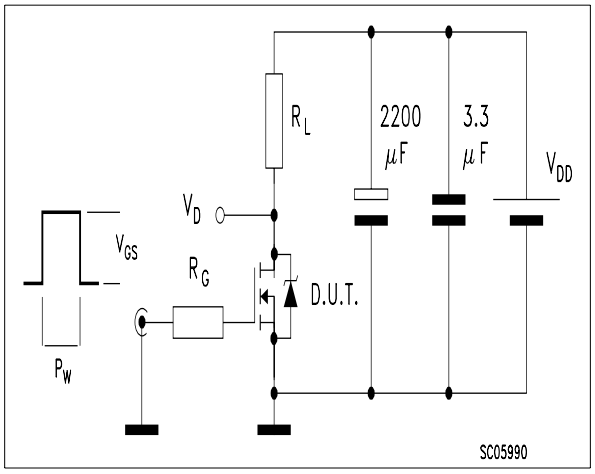


Fig. 4: Gate Charge test Circuit

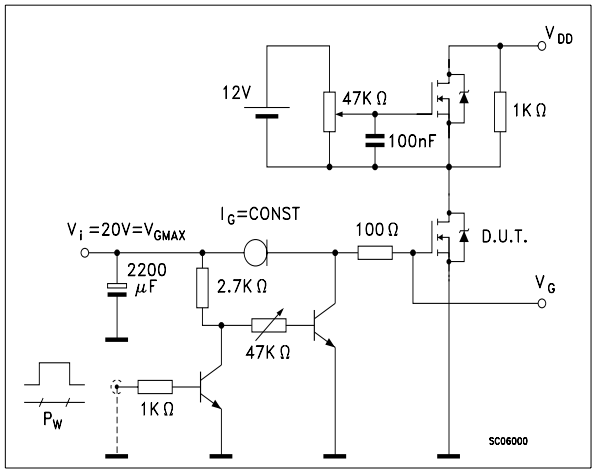
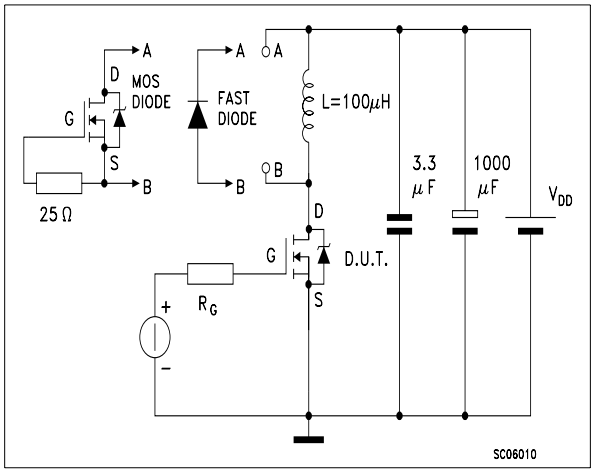


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216